Processor with Asymmetric SIMD Functionality

ABSTRACT

A microprocessor including an execution unit enabled to execute an asymmetric instruction, where the asymmetric instruction includes a set of operand fields and an operation code (opcode). The execution unit is configured to interpret the opcode to perform a first operation on a first set of data indicated by the set of operand fields and to perform a second operation on a second set of data indicated by the set of operand fields, wherein the set of operand fields indicate different sets of data with respect to the first and second operations and further wherein the first and second operations are mathematically different.